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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Appln. Of: TOUNAI

Serial No.: 10/813,834

Filed March 31, 2004

For: METHOD OF TESTING MASK PATTERN AND...

Group: 2624 Confirmation No. 6044

Examiner: PARK, EDWARD DOCKET: NEC A433

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
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TRANSMITTAL LETTER

Dear Sir:

In connection with the above-entitled matter, enclosed please find the following:

1. Appellants' Brief on Appeal; and

2. Credit Card Payment Authorization Form PTO-2038 in the amount of $540.00 to cover the cost of filing the Appeal Brief.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account No. 08-1391.

Respectfully submitted,

Norman P. Soloway
Attorney for Appellant
Registration No. 24,315

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

CERTIFICATE OF MAILING

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By Sharon McKnight

NPS:sm

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

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P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF ON APPEAL

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HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

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HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

TABLE OF CASES

TABLE OF AUTHORITIES

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Appln. Of:	SERVOTTE		
Serial No.:	10/421,623		
Filed:	April 23, 2003		
For:	NON-DAIRY PRODUCTS DERIVED FROM RICE		
Group:	1761	Confirmation No.	5647
Examiner:	CORBIN, Arthur L.	DOCKET:	TIENSE RAFF.35

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Alexandria, VA 22313-1450

APPEAL BRIEF

This Brief is being filed in support of Appellant's Appeal from the Final Rejection by the Primary Examiner to the Board of Appeals and Interferences. A Notice of Appeal was timely filed under Certificate of Mailing on November 26, 2008.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

REAL PARTY IN INTEREST

The Real Party in Interest in this Appeal is NEC Electronics Corporation, a Japanese corporation having its principal place of business at 1753 Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa, Japan. The Application has been assigned to NEC Electronics Corporation, by the inventor Keiichiro Tounai. The Assignment was recorded in the U.S. Patent and Trademark Office on March 31, 2004, at Reel 015175, Frame 0269.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

RELATED APPEALS AND INTERFERENCES

To the best of the knowledge of the undersigned attorney and Appellant, there are no other appeals or interferences that would directly affect, or be directly affected by, or have a bearing on, the Board's decision in the present Appeal.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

STATUS OF THE CLAIMS

Claims 1-26 are pending in the application. Each of these claims are on appeal and are set forth in the **Claims Appendix**.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

STATUS OF AMENDMENTS

A Preliminary Amendment cancelled original claims 1-16 and added new claims 17-48.

Amendment A in response to the July 17, 2007 Office Action amended the specification and drawings as well as claims 1, 8, and 15.

Amendment B in response to the January 29, 2008 Office Action amended claims 8-14 and added new claims 21-26.

Amendment C under Rule 116, Request for Reconsideration and Telephone Interview Summary in response to the July 31, 2008 Final Action made no changes to the claims Amendment C was considered, and discussed in an Advisory Action mailed November 6, 2008.

The Claims Appendix provided herein contains all of the pending claims as amended.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

SUMMARY OF CLAIMED SUBJECT MATTER

A. Background of the Invention

The present invention is directed to a method of testing whether a mask pattern to which optical proximity effect compensation is applied can be a base to form a desired resist pattern. The optical proximity effect is a phenomenon that causes a pattern formed on a resist to differ from a mask pattern from which the pattern in the resist was formed. For example, a width of a line pattern formed on a resist is dependent on an interval between line patterns due to optical proximity effect. Similarly, when a resist is exposed to a light through a mask having an L-shaped pattern, corners of an L-shaped pattern formed in the resist are rounded due to optical proximity effect.

Compensation for optical proximity effect is performed during the design and fabrication of the mask pattern. The mask pattern is modified, taking optical interference into consideration, and tested in order to produce the desired resist pattern. In order to ensure the desired resist pattern, however, it is necessary to test the desired resist pattern by using, for example, computer simulation. Part of the method for determining whether or not the mask pattern adequately compensates for the optical proximity effect requires the determination of sampling points in a predetermined area of the resist pattern and comparing that sampling point to the desired resist pattern.

In testing a mask pattern, it is important to determine a test standard, taking into consideration a structure of a semiconductor integrated circuit as a final product. A test standard is defined in the specification as "a standard in accordance with which a mask pattern is judged as to whether it is accurately formed." (See Specification, p 2, lines 17-19).

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

If accuracy were the sole aim of the test, the test pattern would be constructed with a large number of sampling points in a dense pattern. However, increasing the number of sampling points also increases the amount of processing time required to complete the simulation. Thus, it is necessary to limit the number of sampling points.

B. Summary of the Claimed Invention

The present invention meets the needs discussed above by providing a method of testing a mask pattern, in which an optimized number of sampling points are used for testing a mask pattern, the sampling points having been selected in accordance with a structure of a semiconductor integrated circuit as a final product, ensuring that a mask pattern is accurately tested.

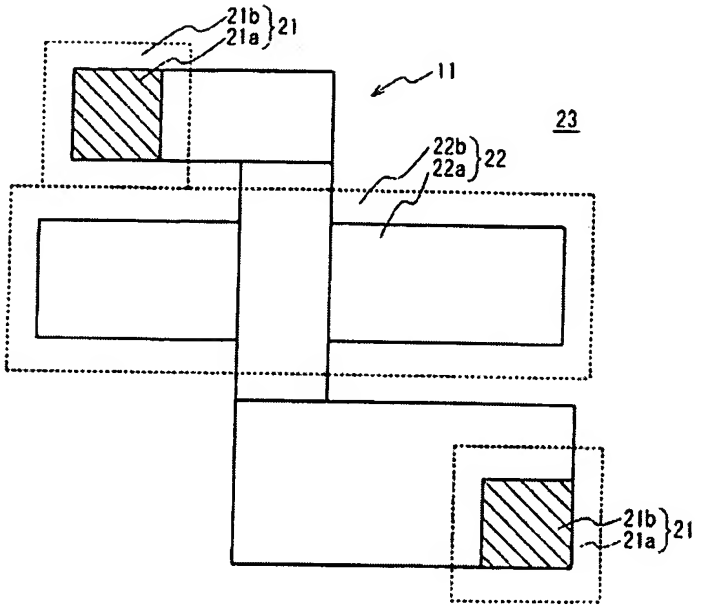
In one aspect of the present invention, as claimed in independent claim 1, there is provided a method of testing a mask pattern by applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, and then forming a mask pattern on the mask layer accordingly. Referring to Fig. 5 of the Specification, reproduced below for convenience, the first pattern (11) is divided into a plurality of areas (21, 22, 23) in accordance with a second pattern to be formed on another mask layer. Sampling points are determined on an edge of the first pattern and a test standard is determined for each of the plurality of areas, wherein the test standard for a first area (21, 22) among said areas and a test standard for a second area (23) among said areas are different from each other. A simulated resist pattern is then formed by exposing the resist to a light through the mask pattern. Finally, the mask pattern is tested by checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within the test standard associated with the

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

area to which the sampling point belongs. (See claim 1; and Specification, p 4, line 28 – p 5, line 10).

FIG.5



By constructing different test standards according to different areas of the first pattern, sampling points may be optimally allocated to areas that will be affected by optical proximity effect and to areas that will be crucial to the function of the resist pattern. Thus, sampling points are determined according to a process that corresponds to a particular area, wherein the processes for determining sampling points in other areas differ from each other. (See claim 2; and Specification, p 5, lines 16-19).

The first pattern may be divided into a plurality of portions along an edge of the first pattern, wherein the test standard is determined for each of the portions. (See claim 3; and Specification, p 5, lines 20-22).

The first pattern may be a pattern for forming a wiring layer, wherein the second pattern may be a pattern for forming a contact reaching the wiring layer. Dimensions of an area in

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

which a contact makes contact with a wiring layer, and an area around the contact area in the designed pattern have to be accurately tested in order to ensure electrical connection in a semiconductor integrated circuit. This is accomplished by including a first area (21, 22) that is a contact area (21) in which the contact makes contact with the wiring layer and an ambient area that surrounds the contact area. (See claims 4-5; and Specification, p 5, lines 23-28, and p 12, lines 24-27).

The first pattern may be a pattern for forming a wiring layer including a gate of a MOS transistor, wherein the second pattern may be a pattern for forming an active area of the MOS transistor. In order to have a MOS transistor in a semiconductor integrated circuit accomplish desired performances, dimensions of a portion acting as a gate of a MOS transistor and around the field layer area in the designed pattern have to be accurately tested. Therefore, the first area (21, 22) including an area (22) obtained by projecting the active area onto the first pattern and an ambient area surrounding the area obtained by projecting the active area onto the first pattern. (See claims 6-7; Specification, p 5, line 29 – p 6, line 4; and p 12, lies 27-30).

The mask layer to be tested may be a gate layer, wherein a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas. Similarly, the number of sampling points in a contact area is higher than the same in other areas. (See claims 21-22; and Specification p 12, line 30 – p 13, line 3).

In another aspect of the present invention, as claimed in independent claim 8 there is provided a computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern. The method of testing a mask pattern in accordance with this aspect of the invention includes each of the steps as outlined above. (See claims 8-14, 23-24; and Specification, p 6, line 5 – p 7, line 9).

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Yet another aspect of the present invention as claimed as independent claim 15, provides a method of forming a mask having a desired mask pattern, according the steps as outlined above for testing a mask pattern. (See claims 15-20, 25-26; and Specification, p 7, line 9 – p 8, line 24).

Thus, the present invention provides a method for testing a mask pattern, a computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern, and a method of forming a mask having a desired mask pattern. Each of these various aspects of the present invention are accomplished, in part, by dividing the pattern to be tested into a plurality of areas in view of a second pattern to be tested, such as a contact or an active area for an MOS transistor, wherein the test standard for each area is distinct from the test standard for any other area.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues on Appeal are:

(a) whether claims 1-3, 8-10, 15-17 and 21-26 are unpatentable under 35 USC §103(a) as being obvious over U.S. Patent No. 5,705,301 to Garza et al. (hereinafter "Garza") in view of US Patent No. 6,453,274 to Kamon, (hereinafter "Kamon");

(b) whether claims 4, 5, 11, 12, 18 and 19 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Garza in view of Kamon, and further in view of U.S. Publication No. 2002/0043615 to Tounai et al. (hereinafter "Tounai"); and

(c) whether claims 6, 7, 13, 14 and 20 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Garza in view of Kamon and further in view of US Patent No. 6,316,163 to Magoshi et al. (hereinafter "Magoshi").

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

ARGUMENT

A. The rejection of claims 1-3, 8-10, 15-17 and 21-26 as obvious over Garza in view of Kamon is in error.

It is well established at law that, for a proper rejection of a claim under 35 USC §103(a) as being obvious based upon a combination of references, the cited combination of references must teach, disclose, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. See, e.g., *In re Dow Chemical*, 5 USPQ 2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 USPQ 871, 881 (CCPA. 1981).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 USC §103(a), then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

1. The combination of Garza and Kamon fail to teach dividing the pattern to be tested into a plurality of areas in accordance with a second pattern to be formed on another mask layer.

The combination of Garza and Kamon do not teach, disclose, or suggest, either implicitly or explicitly all elements of the claims at issue. Specifically, independent claims 1, 8 and 15 require, in part, "dividing said first pattern into a plurality of areas **in accordance with a second pattern to be formed onto another mask layer**." The second pattern is, for example, a pattern for forming a contact, an active area of an MOS transistor, or some other pattern for forming a device that will interface with the designed resist pattern. (See

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Specification, p 5, line 23 – p 6, line 4). Thus, the areas of the first pattern are divided according to the functionality of the resist as it interfaces with other devices.

The Examiner mistakenly cites Garza as teaching dividing the pattern to be tested into a plurality of areas in accordance with a second pattern to be formed onto another mask layer. Garza does divide the pattern into a plurality of areas, but this division is not performed in accordance with a second pattern to be formed onto another mask layer. The portions of Garza cited by the Examiner clearly describe the division of the layout into a grid regions. (See Garza col. 8, lines 41-62). As is clearly shown by Fig. 5B of Garza, also cited by the Examiner, (see below), the grid (520) is purely geometric and clearly does was not chosen in accordance with a second pattern to be formed on another mask layer.[1]

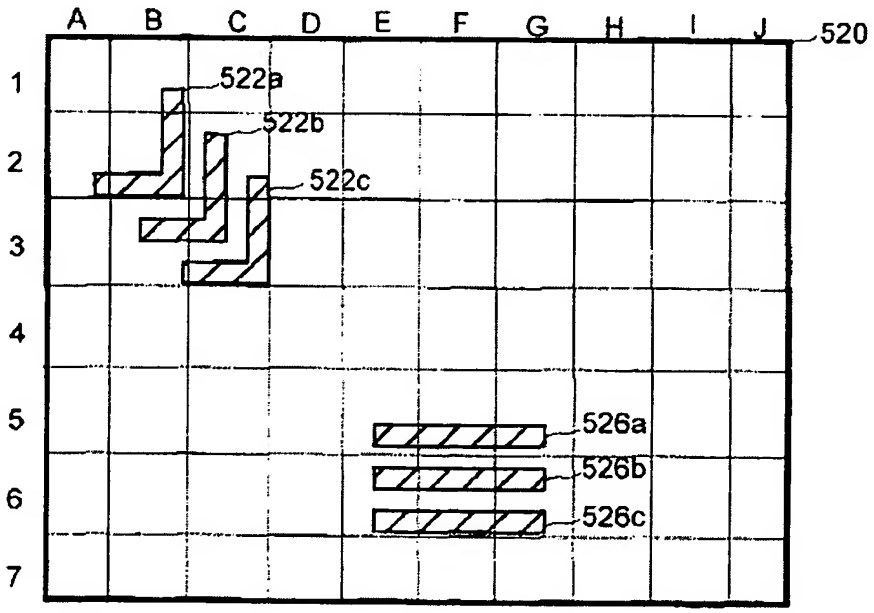


FIG. 5B

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

[1] The other areas shown in Fig. 5B (522a, 522b, 522c, 526a, 526b, 526c) represent features of the mask pattern.

Furthermore, Garza states that the purpose of the grid system is to enable dividing a complex optical proximity correction problem into small and simpler segments, and that it is not necessary to the practice of the invention. (See Garza col. 11, lines 36-39). One having ordinary skill in the art could not infer from Garza any teaching or rationale that would modify the row and column grid of Garza to correspond to a second pattern where there is no mention of a second pattern and the purpose of the grid section is clearly stated as merely dividing the problem into smaller segments.

The Kamon reference fails to supply the missing teachings of Garza. Fig. 6 of Kamon displays a division of the pattern into a grid to allow optical proximity correction to occur separately in each block. (Kamon, col. 6, lines 34-38). As with Garza, there is no teaching that would allow one having ordinary skill in the art to conclude that it is obvious from Kamon to divide the design into a plurality of blocks in accordance with a second design.

Both Garza and Kamon fail to teach dividing the first pattern into a plurality of areas in accordance with a second pattern to be formed onto a mask layer as required by each of independent claims 1, 8, and 15. Thus, no combination of Garza and Kamon can achieve or render obvious any of claims 1, 8, and 15, and claims 2, 3, 9, 10, 16, 17, and 21-26 that depend thereon.

2. The combination of Garza and Kamon fail to teach the application of a first test standard to a first area and of a second test standard to a second area, wherein the first test standard and the second test standard differ from each other.

In addition to the deficiencies discussed above, Garza and Kamon fail to teach all of the limitations of independent claims 1, 8 and 15, which require, in part, "dividing said first pattern into a plurality of areas . . . **wherein a test standard for a first area among said areas and a**

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

test standard for a second area among said areas are different from each other." The Specification defines the test standard as "**a standard in accordance with which a mask pattern is judged as to whether it is accurately formed.**" (See Specification, p 2, lines 17-19). The claims therefore require that distinct areas of the first pattern will be associated with different standards for judging the accuracy of the mask pattern.

The Examiner admits that Garza does not teach this feature. In fact, the Examiner admits that Garza does not teach a test standard of any kind. (Final Action, p 3). Instead, the Examiner erroneously relies on Kamon to teach this feature. In the Final Action, the Examiner blindly points to figure 5, numeral s6, and column 5, lines 14-47, as containing this teaching. Fig. 5, shown below, includes the step (s6) of determining if the correction amount is within an allowable range. The "allowable range" of Kamon could be defined as a standard in accordance with which a mask pattern is judged as to whether it is accurately formed. However, there is no statement in the four corners of Kamon that would allow one having ordinary skill in the art to infer that the "allowable range" of Kamon is anything but a constant. This reading of the term "allowable range" is further supported by the detailed description of Kamon (at col. 5, lines 33-40), which states:

> Then the determination unit 7 determines whether the correction amount is within the predefined allowable range (step S6). If the correction amount is not within the allowable range, it is considered that the correction is not good enough, and thus the process returns to step S2 so as to calculate the projection image again and correct the data again in steps S3 to S5. Steps S2 to S6 are performed repeatedly **until the correction value falls within the allowable range.**

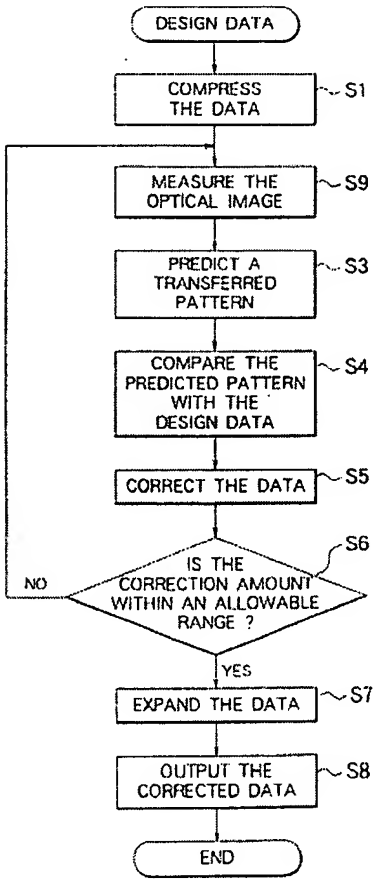
Wherein the Kamon states that the process continues "repeatedly until the correction value falls within the allowable range," one having ordinary skill in the art would have to conclude that

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

the allowable range was a constant. In the absence of any discussion of how to compensate for a moving range to reach a definitive conclusion, no other reading makes sense.

FIG. 5



The passage cited by the Examiner in the Final Action also discusses a correction amount that is used to change the compressed data (s2) used to create and change the optical image of the pattern with each iterative step. (See Fig. 3, Kamon col. 5, lines 14-47). The correction amount does change with each iteration, (thereby making a first and second correction amount according to the Examiner's reasoning), but does not meet the definition of a test standard. The correction amount is used to change the optical image (an input) and is not

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

used as a standard for judging the accuracy of formation of a mask pattern. Rather, the correction amount is the result of a comparison of the pattern formed with the allowable range.

In the Advisory Action mailed November 6, 2008, the Examiner further muddles the issues by noting that the correction data may be different for distinct areas of the pattern. (Advisory Action, p 2-3). Having established above that the correction amount of Kamon does not meet the definition of a test standard according to the claimed invention, the Examiner's arguments have no merit.

Further, the Examiner contends that the division of the pattern of Kamon into a grid pattern makes it **possible** to perform different test standards on different data blocks. (See Advisory Action, p 2-3). The expression of the possibility of accomplishing the claimed invention does not support a prima facie case of obviousness and demonstrates the hindsight used by the Examiner. Conclusory statements are insufficient to support a rejection without some explicit analysis to support the conclusion of obviousness. *KSR Intern. Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007), *quoting In re Kahn*, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006). Moreover, because the grid pattern shown in Fig. 6 of Kamon is divided only to allow parallel solution of the problem, one having ordinary skill in the art would necessarily conclude that the standard for judging the accuracy of the pattern formed would by the same for all data blocks of Kamon. Therefore, the grid of Kamon reinforces the explicit teaching of a single test standard to be applied to the entire pattern.

Thus, the combination of Kamon and Garza cannot achieve or render obvious any of claims 1, 8, and 15, nor any of claims 2, 3, 9, 10, 16, 17, and 21-26 that depend thereon.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

B. The rejection of claims 4, 5, 11, 12, 18 and 19 under 35 U.S.C. § 103(a) as obvious over Garza in view of Kamon, and further in view of Tounai is in error.

Claims 4, 5, 11, 12, 18 and 19 also depend from claims 1, 8 or 15, as the case may be. The deficiencies of the combination of Garza and Kamon are described above. Tounai does not overcome these deficiencies.

Tounai is cited by the Examiner as teaching a first pattern for forming a wiring layer, a second pattern for forming a contact reaching said wiring layer, and an area of the pattern that includes the contact area. (Final Action, p 10). Even assuming arguendo that Tounai is as the Examiner states, Tounai does not supply the missing teachings of Garza and Kamon.

Thus, claims 4, 5, 11, 12, 18, and 19 are allowable over the art for the same reasons above adduced relative to claims 1, 8 and 15, as well as for their own additional limitations.

C. The rejection of claims 6, 7, 13, 14 and 20 under 35 USC §103(a) as being unpatentable over Garza in view of Kamon and further in view of Magoshi is in error.

Claims 6, 7, 13, 14 and 20 are dependent on claims 1, 8 or 15, as the case may be. The deficiencies of the combination of Garza et al. and Kamon are discussed above. Magoshi et al. fails to supply the missing teachings.

Magoshi is cited by the Examiner as teaching a first pattern for forming a wiring layer including the gate of a MOS transistor, a second pattern for forming an active area of said MOS transistor, and an area of the pattern that is obtained by projecting the said active area onto said first pattern. (Final Action, p 10). Even assuming arguendo that Magoshi is as the Examiner states, Magoshi does not supply the missing teachings of the Garza and Kamon combination.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Thus, claims 6, 7, 13, 14 and 20 are allowable for the same reasons above adduced relative to claims 1, 8 and 15, as well as for their own additional limitations.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

SUMMARY

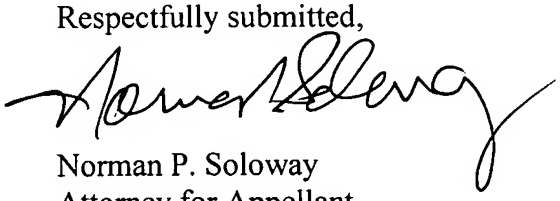
In summary, the Examiner has failed to present a prima facie case of obviousness for any of the claims in question. In particular, the Examiner has failed to consider specific claim limitations, and the Examiner has misapplied the prior art by equating the correction amount of Kamon with the test standard of the present invention, where the correction amount does not fit the definition of a test standard given by the specification.

Accordingly, it is submitted that claims 1, 8, and 15, and the several claims that depend thereon, cannot be said to be obvious from the combination of Garza and Kamon alone or in combination with Tounai and Magoshi. As the Examiner has failed to make out a prima facie case of obviousness, Appellants respectfully submit that the rejection of the claims is in error and should be reversed.

CONCLUSION

In view of the foregoing, it is respectfully requested that the rejection of the subject application be reversed in all respects.

Respectfully submitted,



Norman P. Soloway
Attorney for Appellant
Reg. No. 24,315

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

CERTIFICATE OF MAILING

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By: Sharon McKnight

NPS:RAM

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

CLAIMS APPENDIX

Claim 1 (previously presented): A method of testing a mask pattern, comprising the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other.

Claim 2 (original): The method as set forth in claim 1, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ---), and first to N-th processes are different from one another.

Claim 3 (original): The method as set forth in claim 1, further comprising:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Claim 4 (original): The method as set forth in claim 1, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

Claim 5 (original): The method as set forth in claim 4, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

Claim 6 (original): The method as set forth in claim 1, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Claim 7 (original): The method as set forth in claim 6, wherein said fourth area is comprised of said fifth area and an ambient area surrounding said fifth area.

Claim 8 (previously presented): A computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern, wherein said method is executed by said computer in accordance with said program including the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other.

Claim 9 (previously presented): The computer-readable medium storing a program as set forth in claim 8, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ---), and first to N-th processes are different from one another.

Claim 10 (previously presented): The computer-readable medium storing a program as set forth in claim 8, wherein said steps further include:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Claim 11 (previously presented): The computer-readable medium storing a program as set forth in claim 8, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

Claim 12 (previously presented): The computer-readable medium storing a program as set forth in claim 11, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

Claim 13 (previously presented): The computer-readable medium storing a program as set forth in claim 8, wherein said first pattern is a pattern for forming a wiring layer including a

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Claim 14 (previously presented): The computer-readable medium storing a program as set forth in claim 13, wherein said fourth area is comprised of said fifth area and an ambient area surrounding said fifth area.

Claim 15 (previously presented): A method of forming a mask having a desired mask pattern, including the steps of :

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern;

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs; and

(g) transferring said mask pattern onto a mask,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

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MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Claim 16 (original): The method as set forth in claim 15, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ---), and first to N-th processes are different from one another.

Claim 17 (original): The method as set forth in claim 15, further comprising:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Claim 18 (original): The method as set forth in claim 15, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

Claim 19 (original): The method as set forth in claim 18, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

Claim 20 (original): The method as set forth in claim 15, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Claim 21 (previously presented): The method as set forth in claim 1, wherein said mask layer to be tested is a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas.

Claim 22 (previously presented): The method as set forth in claim 1, wherein said mask layer to be tested is a gate layer, and a number of sampling points in a contact area is higher than the same in other areas.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

Claim 23 (previously presented): The computer-readable medium storing a program as set forth in claim 8, wherein said mask layer to be tested is a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas.

Claim 24 (previously presented): The computer-readable medium storing a program as set forth in claim 8, wherein said mask layer to be tested is a gate layer, and a number of sampling points in a contact area is higher than the same in other areas.

Claim 25 (previously presented): The method as set forth in claim 15, wherein said mask layer to be tested is a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas.

Claim 26 (previously presented): The method as set forth in claim 15, wherein said mask layer to be tested is a gate layer, and a number of sampling points in a contact area is higher than the same in other areas.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

EVIDENCE APPENDIX

NOT APPLICABLE

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

RELATED PROCEEDINGS APPENDIX

NOT APPLICABLE

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567